memory architecture, a uniform memory architecture, and an input/output intensive workload.

11. The processor of claim **1**, further comprising a user interface to receive at least one EPB value from a user.

12. The processor of claim **11**, wherein the at least one EPB value is to be provided based at least in part on a time of day policy.

13. A machine-readable medium having stored thereon instructions, which if performed by a machine cause the machine to perform a method comprising:

receiving an energy performance bias (EPB) value in power control logic of a processor from a plurality of threads executing on the processor and determining a global EPB value based at least in part on the EPB value received from the plurality of threads, the EPB value to indicate a preference of a user for a tradeoff between power optimization and performance optimization;

accessing a table based on the global EPB value; and

updating at least one setting of a power management feature controlled by the power control logic based on information obtained from the table.

14. The machine-readable medium of claim **13**, wherein the method further comprises selecting a bin of a plurality of bins, each associated with a power-performance profile using the global EPB value.

15. The machine-readable medium of claim **13**, wherein the method further comprises providing an interface to enable a user, an operating system or a baseboard management controller to set the EPB value, and controlling a plurality of power management features via input of the EPB value.

16. The machine-readable medium of claim **13**, wherein the method further comprises receiving the EPB value with a first value for a first portion of a day and with a second value for a second portion of the day, wherein the first value is to configure a system for first performance during the first portion of the day corresponding to peak user hours, and the second value to configure the system for higher power savings during the second portion of the day corresponding to non-peak user hours.

17. A system comprising:

a multicore processor including a plurality of cores, at least one cache memory and a memory controller;

a tuning circuit to dynamically select a balance between power consumption and performance based on an energy performance bias (EPB) value, wherein the tuning circuit is to access an entry of a tuning table based at least in part on the EPB value and a workload configuration value and update a setting for a power management feature responsive to a value stored in a field of the entry, wherein the workload configuration value is to indicate a predominant workload type to be executed on the system, the tuning table including a first set of entries associated with a first workload type and a second set of entries associated with a second workload type; and

a system memory coupled to the processor via a memory interconnect.

18. The system of claim **17**, wherein tuning circuit is to update at least one setting of a first power management feature controlled by a power control logic of the multicore processor, the at least one setting obtained from a field of an entry of the tuning table associated with a bin in which the EPB value is included.

19. The system of claim **18**, wherein multicore processor comprises the tuning circuit.

20. The system of claim **17**, wherein the multicore processor comprises a power control logic, the power control logic comprising the tuning circuit, wherein the tuning circuit is to generate a bin value from the EPB value and access the tuning table using the bin value.

* * * * *